Multi-Temp SATA SSD 2.5”

Memoright

Product Data Sheet

STM Plus

SATAIII-6.0 Gb/s

Commercial, Industrial & Semi-industrial Temperature Grade

Revision: V04

Date: October 2013

Multi-Temp SATA Solid State Drive 2.5” – STM Plus Series

32 GB~256 GB

1. Features

- **Form Factor**
  - 2.5” SATA solid State Drive (SSD)
  - 100 mm x 69.85 mm 9.5 mm
  - Totally compliant to standard SATA hard disk drive
  - 7+15 pin (SATA power) SATA connector
- **Available Capacities**
  - 32 GB~256 GB (MLC NAND Flash)
- **ECC**
  - BCH 40 bits ECC
- **High Performance**
  - Up to 600 MB/s burst transfer rate in SATAIII, 6 Gb/s (NCQ Supported)
  - Sustained Read Performance: up to 500 MB/s
  - Sustained Write Performance: up to 460 MB/s
  - 4KB Random Read/Write IOPS up to : 70000/35000 (peak value)
- **High Reliability**
  - MTBF > 2,100,000 hours
  - Endurance: In normal operation condition, guarantees for 3 years product lifetime for half the SSD capacity sequential write per day.
  - Dynamic, static and active balanced wear-leveling strategy
  - Bad-Block Management
  - S.M.A.R.T support
- **Temperature Ranges**
  - Commercial Temperature Range: 0℃ ~+70℃
  - Semi-industrial Temperature Range: -20℃ ~+70℃
  - Industrial Temperature Range: -40℃ ~+85℃

2. Contents

3. Ordering Information

The following Table 1 lists the part No. for Memoright STM Plus series SSDs.

Table 1: Commercial temperature product list

Part Number	Capacity	Flash Type	Form Factor
MRSAJ9A032GK125C00	32 GB*	MLC	2.5”
MRSAJAA064GK225C00	64 GB*	MLC	2.5”
MRSAJAA128GK225C00	128 GB*	MLC	2.5”
MRSAJAA256GK225C00	256 GB*	MLC	2.5”

Part Number	Capacity	Flash Type	Form Factor
MRSAJ9A032GTT25C00	32 GB*	MLC	2.5”
MRSAJAA064GTW25C00	64 GB*	MLC	2.5”
MRSAJAA128GTW25C00	128 GB*	MLC	2.5”
MRSAJAA256GTW25C00	256 GB*	MLC	2.5”

Table 2: Semi-industrial temperature product list

Part Number	Capacity	Flash Type	Form Factor
MRSAJ9A032GK125S00	32 GB*	MLC	2.5”
MRSAJAA064GK225S00	64 GB*	MLC	2.5”
MRSAJAA128GK225S00	128 GB*	MLC	2.5”
MRSAJAA256GK225S00	256 GB*	MLC	2.5”

Part Number	Capacity	Flash Type	Form Factor
MRSAJ9A032GTT25S00	32 GB*	MLC	2.5”
MRSAJAA064GTW25S00	64 GB*	MLC	2.5”
MRSAJAA128GTW25S00	128 GB*	MLC	2.5”
MRSAJAA256GTW25S00	256 GB*	MLC	2.5”

Table 3 Industrial temperature product list

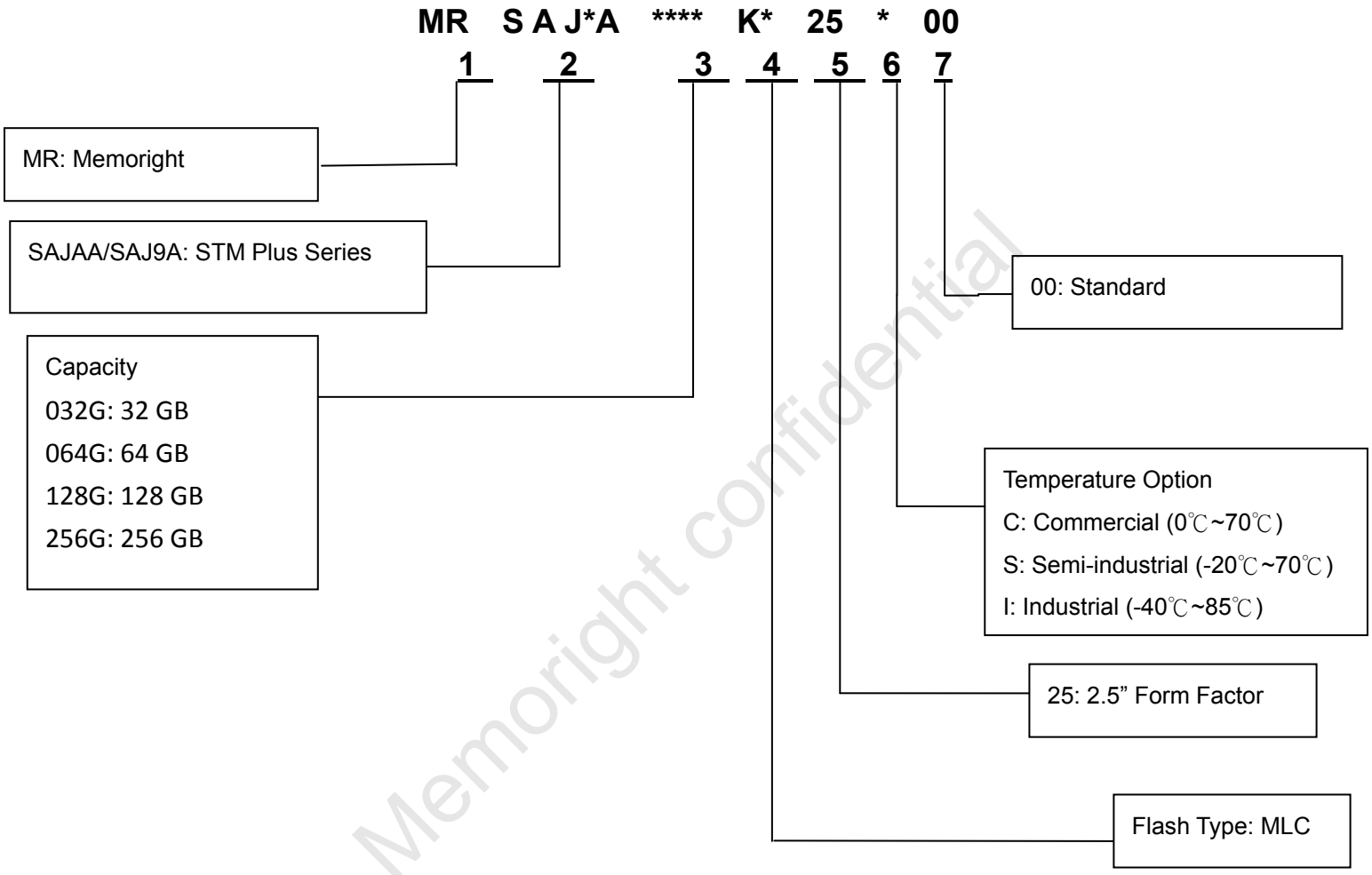
Part Number	Capacity	Flash Type	Form Factor
MRSAJ9A032GTT25I00	32 GB*	MLC	2.5”
MRSAJAA064GTW25I00	64 GB*	MLC	2.5”
MRSAJAA128GTW25I00	128 GB*	MLC	2.5”
MRSAJAA256GTW25I00	256 GB*	MLC	2.5”

* 1 GB=1,000,000,000 Bytes

For latest ordering information, please consult Memoright’s sales representatives or check on our website:

http://www.memoright.com

3.1 Part Number Decoder



4. General Description

The Memoright STM Plus series SSD provides you ultimate performance and ultra-high reliability over traditional hard disk drive by achieving up to 500 MB/s/460 MB/s sequential read/write rate and integrated protection technologies such as bad block management, wear-leveling. The above-mentioned features made Memoright STM Plus series SSD the best solution for various consumer electronics and industrial applications.

For reliability, Memeoright STM Plus series SSD integrates **dynamic, static and active (inactive) balanced wear leveling technology** to ensure an equal usage of the Flash memory cells to extend the SSD life time. Moreover, it provides features such as Enhanced **ECC algorithm**, **bad block management algorithm and MTBF>2,100,000** hours to assure overall reliability.

Memoright STM Plus series SSD consists solely of semiconductor devices, which means it doesn't have any mechanical part such as platter (disk), motor and suspension as traditional hard disk drive. Its characteristics such as high performance, capacity, reliability, ruggedness, low power consumption and small form factor make it the best storage solution not only for portable computing devices such as Tablet PC and UMPC but also for industrial application with extreme environment and increased MTBF requirements. Due to Memoright STM Plus series' SATA interface and 2.5" form factor, it is the best solution to replace traditional 2.5" HDD.

4.1 Physical Description

The important component of Memoright STM Plus SSD includes a Flash controller and NAND Flash memory modules. The controller works with a host system to allow data to be written to and read from the Flash memory modules through a (SATA) interface. The SSD is offered in a 2.5" form factor with a SATA connector.

4.2 System Performance

Table 4: System Performance Table

System Performance		Max.	Unit
Data transfer Rate (SATA burst (6 Gb/s)		600	MB/s
Sustained Sequential Read Rate	32 GB	400	MB/s
Sustained Sequential Write Rate	32 GB	100	MB/s
Sustained Sequential Read Rate	64 GB	500	MB/s
Sustained Sequential Write Rate	64 GB	180	MB/s
Sustained Sequential Read Rate	128 GB	500	MB/s
Sustained Sequential Write Rate	128 GB	300	MB/s
Sustained Sequential Read Rate	256 GB	500	MB/s
Sustained Sequential Write Rate	256 GB	460	MB/s

*1 GB=1024 Mega Bytes

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Value
Commercial Operating Temperature	0℃ to 70℃
Semi-industrial Operating Temperature	-20℃ to 70℃
Industrial Operating Temperature	-40℃ to 85℃
Temperature Gradient (℃ per hour max, non-condensing)	20℃ (operating)
Temperature Gradient (℃ per hour max, non-condensing)	30℃ (non-operating)
Power Supply Voltage Range	5V DC ± 5%

4.3.2 Power Consumption (*)

Table 6: Power Consumption

Current/Power Consumption	5V	Unit
Input Current (Max.)	1.3	A
Continue Read Power (Average)	1	W
Continue Write Power (Average)	2	W
Idle Mode Power (Average)	0.5	W

* All values are tested under room temperature 25℃ @ 5V. The power consumption may vary depends on different platform, OS, BIOS & test tools.

4.3.3 Recommended Storage Conditions

Table 7: Recommended Storage Conditions

Parameter	Value
Commercial & Semi-industrial Storage Temperature	-40℃ to 85℃
Industrial Storage Temperature	-55℃ to 95℃

4.3.4 Shock, Vibration and Humidity

Table 8: Shock, Vibration and Humidity

Parameter	Value
Humidity (non-condensing)	5%~95% (Operating)
Relative Humidity Gradient	30% per hour max
Vibration	10G (Peak, 10~2000Hz)
Shock (Operating)	50G, (11ms duration, half sine wave)
Shock (Non-Operating)	1500G, (0.5ms duration, half sine wave)

4.4 Reliability

Table 9: Reliability

Parameter	Value
Mean Time Between Failures (MTBF)	＞ 2,100,000 hours (Calculation mode: Telcordia SR-332 Issue 1 Method 1, Case 1)
Data Retention	10 years

4.5 Physical Dimensions

Physical Dimensions		Unit
Length	100	mm
Width	69.85	mm
Thickness	9.5	mm

4.6 CHS Parameter

Unformatted Capacity	Guaranteed Sectors	Bytes per Sector
32 GB*	62533296	512
64 GB*	117231408	512
128 GB*	234441648	512
256 GB*	468862128	512

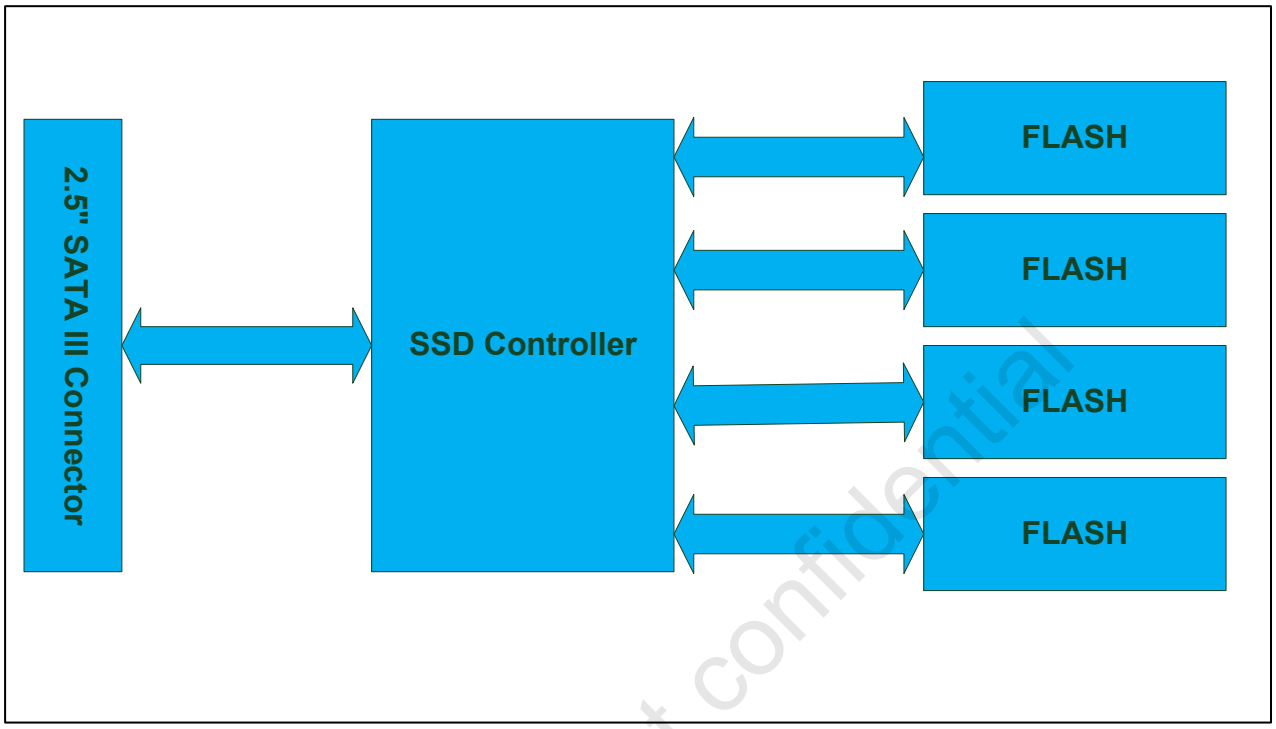
*1GB=1,000,000,000 Bytes

4.7 Drive Geometry

Capacity	Default Cylinders	Default Heads	Default Sectors
32 GB*	62037	16	63
64 GB*	116301	16	63
128 GB*	232581	16	63
256 GB*	465141	16	63

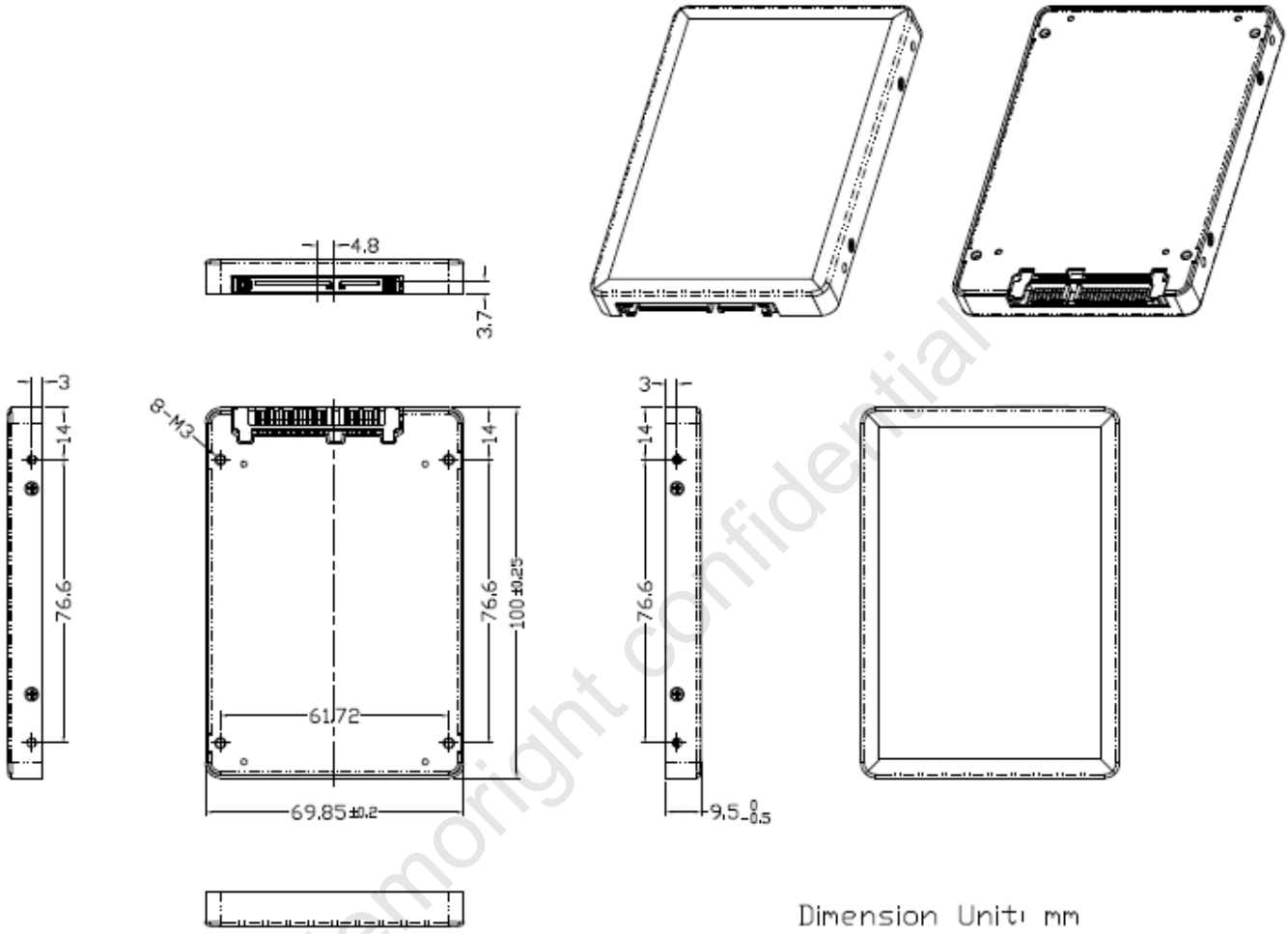
5. Functional Block Diagram

Figure 1: Functional Block Diagram



6. Physical Dimension Diagram

Figure 2: Physical Dimension Diagram



Physical Dimensions		Unit
Length	100	mm
Width	69.85	mm
Thickness	9.5	mm

7. Electrical Interface

7.1 Electrical Description

The drive uses the industry-standard Serial ATA interface that supports 16-bit data transfers. It supports programmed input/output (PIO) modes 0–4; Ultra DMA modes 0–6. The drive also supports the use of the IORDY signal to provide reliable high-speed data transfers.

For detailed information about the Serial ATA interface, refer to the draft of AT Attachment with Packet Interface Extension (ATA-8), NCITS T13 1410D Standards.

The connector on Memoright STM Plus Series is divided into a signal Segment and a power Segment. The following tables summarize the signals on the SATA interface connector. For a detailed description of these signals, refer to the Draft ATA-8 Standard.

Figure 3 SATA pin

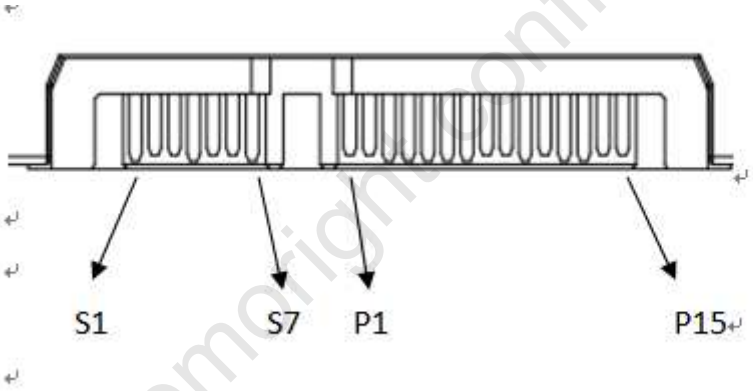


Table 10 Pin Assignment and description for Signal and Power pins

Pin Name	Signal Name	Description
S1	Ground	Second Mate
S2	R+	+Differential Receive Signal
S3	R-	-Differential Receive Signal
S4	Ground	Second Mate
S5	T-	-Differential Transmit Signal
S6	T+	+Differential Transmit Signal
S7	Ground	Second Mate
Pin Name	**Signal Name**	**Description**
P1, P2,P3	V3.3	3.3V Power(Not used)
P4	Ground	First Mate
P5	Ground	Second Mate
P6	Ground	Second Mate
P7	V5	5V power, pre-charge, second Mate
P8	V5	5V power
P9	V5	5V power
P10	Ground	Second Mate
P11	Reserved	Reserved
P12	Ground	First Mate
P13	V12	12V Power(Not used)
P14	V12	12V Power(Not used)
P15	V12	12V Power(Not used)

8. Feature Descriptions

8.1 Wear Leveling

For extending SSD's life time, a sophisticated wear leveling technology is important. Memoright STM Plus series provides dynamic, static (initiative) balanced wear leveling strategy. The dynamic wear leveling algorithm ensures that erase/write cycles can be evenly distributed across all flash memory block locations to prevent excessive writes to the same physical flash memory location.

8.2 Bad Block Management

Memorigt STM Plus series SSD provides bad block management function with a certain number of reserved blocks. When a user data block fails, a reserved block will replace the failed block. The replacement of bad block is transparent to user.

8.3 Endurance

In normal operation condition, guarantees for 3 years product lifetime for half the SSD capacity sequential write per day.

8.4 ECC

The SSD provides Enhanced ECC algorithm which reduces error rate and enforces write endurance at the same time. There are two kinds of ECC algorithm as follows.
BCH 40: it detects and corrects 40 random bits per 1024 Bytes.

8.5 Standards Compliance

Memoright STM Plus SSD complies with following standards.
FCC
CE
RoHS

9. Supported ATA Commands

Memoright STM Plus series SSD supports ATA commends that is shown as following table. For details of the ATA command, please refer to the Draft ATA-8 Standard.

Table 11 Supported ATA Commands

Feature Set	ATA-8 Reference	Mandatory / Optional	Support
General feature set	4.2	**M**	YES
48-Bit Address feature set	4.4	O	YES
General Purpose Logging (GPL) feature set	4.10	O	YES
Host Protected Area (HPA) feature set	4.11	O	YES
Native Command Queuing (NCQ) feature set	4.15	O	YES
Power Management feature set	4.18	**M**	YES
Security feature set	4.20	O	YES
S.M.A.R.T. feature set	4.21	O	YES
Software Settings Preservation (SSP) feature set	4.22	O	YES
Key: M – Mandatory, O – Optional, P – Prohibited, N – Not defined			

Table 12 Supported ATA Commands (Sorted Alphabetically)

Commands	Feature Set	ATA-8	Comments	OpCode
CHECK POWER MODE	Power Mgmt	M		E5h
DATA SET MANAGEMENT EXT (I.E. TRIM)	Data Set Mgmt	O		06h
DISABLE AUTOMATIC ACOUSTIC MGMT	Set Features			EFh
DISABLE DEVICE-INITIATED INTERFACE POWER-STATE TRANSITIONS	Set Features			EFh
DISABLE DMA SETUP FIS AUTO-ACTIVATE OPTIMIZATION	Set Features			EFh
DISABLE LOOK-AHEAD	Set Features			EFh
DISABLE REVERTING TO POWER-ON DEFAULTS	Set Features			EFh
DISABLE SOFTWARE SETTINGS PRESERVATION	Set Features			EFh

DISABLE WRITE CACHE	Set Features		EFh
DOWNLOAD MICROCODE	General	O	92h
ENABLE AUTOMATIC ACOUSTIC MGMT	Set Features		EFh
ENABLE DEVICE-INITIATED INTERFACE POWER-STATE TRANSITIONS	Set Features		EFh
ENABLE DMA SETUP FIS AUTO-ACTIVATE OPTIMIZATION	Set Features		EFh
ENABLE LOOK-AHEAD	Set Features		EFh
ENABLE REVERTING TO POWER-ON DEFAULTS	Set Features		EFh
ENABLE SOFTWARE SETTINGS PRESERVATION	Set Features		EFh
ENABLE WRITE CACHE	Set Features		EFh
EXECUTE DEVICE DIAGNOSTIC	General	M	90h
FLUSH CACHE	General	M	E7h
FLUSH CACHE EXT	48-bit Address	M	EAh
IDENTIFY DEVICE	General	M	ECh
IDLE	Power Mgmt	M	E3h
IDLE IMMEDIATE	Power Mgmt	M (No support for unload)	E1h
INITIALIZE DEVICE PARAMETERS	General	M	91h
NOP	General	O	00h
READ BUFFER	General	O	E4H
READ DMA	Data Transfer	M	C8h
READ DMA (w/o retry)	Data Transfer	Obs	C9h
READ DMA EXT	48-bit Address	M	25h
READ FPDMA QUEUED	Data Transfer NCQ	M	60h
READ LOG DMA EXT	Gen.Purpose Logging 48-bit	O	47h
READ LOG EXT	Gen.Purpose Logging	M	2Fh
READ LONG	Data Transfer		22h
READ LONG without Retry	Data Transfer		23h

READ MULTIPLE	Data Transfer	M	C4h
READ MULTIPLE EXT	48-bit Address	M	29h
READ NATIVE MAX ADDRESS	HPA	M	F8h
READ NATIVE MAX ADDRESS EXT	HPA	M	27h
READ SECTOR(S)	Data Transfer	M	20h
READ SECTOR(S) EXT	48-bit Address	M	24h
READ SECTOR(S) without Retry	Data Transfer		21h
READ VERIFY SECTOR(S)	General	M	40h
READ VERIFY SECTOR(S) EXT	48-bit Address	M	42h
READ VERIFY SECTORS(S) (w/o retry)	General	Obs	41h
RECALIBRATE	General	Obs	10h
SCT COMMAND / STATUS	S.M.A.R.T.		B0h
SCT DATA TABLES: READ TABLE: (HDA) TEMPERATURE HISTORY TABLE	S.M.A.R.T.		B0h
SCT DATA TRANSFER	S.M.A.R.T.		B0h
SCT FEATURE CONTROL: FORCED WRITE CACHE ENABLE & DISABLE	S.M.A.R.T.		B0h
SCT WRITE SAME	S.M.A.R.T.	Not recommended for SSDs; can negatively affect initial performance of drive.	B0h
SECURITY DISABLE PASSWORD	Security	M	F6h
SECURITY ERASE PREPARE	Security	M	F3h
SECURITY ERASE UNIT	Security	M	F4h
SECURITY FREEZE LOCK	Security	O	F5h
SECURITY SET PASSWORD	Security	M	F1h
SECURITY UNLOCK	Security	M	F2h
SEEK	General	M	70h
SET MAX ADDRESS	HPA	M	F9h
SET MAX ADDRESS EXT	HPA	M	37h
SET MAX FREEZE LOCK	HPA	O	F9h/04h
SET MAX LOCK	HPA	O	F9h/02h

SET MAX SET PASSWORD	HPA	O	F9h/01h
SET MAX UNLOCK	HPA	O	F9h/03h
SET MULTIPLE MODE	General	M	C6h
SET TRANSFER MODE (based on value in SECTOR COUNT REGISTER)	Set Features		EFh
SLEEP	Power Mgmt	M	E6h
S.M.A.R.T. ABORT OFFLINE ROUTINE	S.M.A.R.T.		B0h
S.M.A.R.T. DISABLE OPERATIONS	S.M.A.R.T.	M	B0h/D9h
S.M.A.R.T. ENABLE OPERATIONS	S.M.A.R.T.	M	B0h/D8h
S.M.A.R.T. ENABLE/DISABLE AUTOSAVE	S.M.A.R.T.	M	B0h/D2h
S.M.A.R.T. EXECUTE CONVEYANCE SELF-TEST ROUTINE (captive)	S.M.A.R.T.		B0h
S.M.A.R.T. EXECUTE CONVEYANCE SELF-TEST ROUTINE (offline)	S.M.A.R.T.		B0h
S.M.A.R.T. EXECUTE EXTENDED SELF-TEST ROUTINE	S.M.A.R.T.		B0h
S.M.A.R.T. EXECUTE EXTENDED SELF-TEST ROUTINE (captive)	S.M.A.R.T.		B0h
S.M.A.R.T. EXECUTE OFFLINE IMMEDIATE	S.M.A.R.T.	O	B0h/D4h
S.M.A.R.T. EXECUTE OFFLINE ROUTINE	S.M.A.R.T.		B0h
S.M.A.R.T. EXECUTE SELECTIVE SELF-TEST ROUTINE	S.M.A.R.T.		B0h
S.M.A.R.T. EXECUTE SELECTIVE SELF-TEST ROUTINE (captive)	S.M.A.R.T.		B0h
S.M.A.R.T. EXECUTE SHORT SELF-TEST ROUTINE	S.M.A.R.T.		B0h
S.M.A.R.T. EXECUTE SHORT SELF-TEST ROUTINE (captive)	S.M.A.R.T.		B0h
S.M.A.R.T. READ DATA	S.M.A.R.T.	O	B0h/D0h
S.M.A.R.T. READ LOG	S.M.A.R.T.	O	B0h/D5h
S.M.A.R.T. READ THRESHOLD	S.M.A.R.T.	Obs	B0h-D1h

S.M.A.R.T. RETURN STATUS	S.M.A.R.T.	O	B0h/DAh
S.M.A.R.T. SAVE ATB THRESHOLDS	S.M.A.R.T.	Obs	B0h-D3h
S.M.A.R.T. WRITE LOG	S.M.A.R.T.	O	B0h/D6h
STANDBY	Power Mgmt	M	E2h
STANDBY IMMEDIATE	Power Mgmt	M	E0h
WRITE BUFFER	General	O	E8h
WRITE DMA	Data Transfer	M	CAh
WRITE DMA (w/o retry)	Data Transfer	Obs	CBh
WRITE DMA EXT	48-bit Address	M	35h
WRITE DMA FUA EXT	48-bit Address	M	3Dh
WRITE FPDMA QUEUED	Data Transfer NCQ	M	61h
WRITE LOG DMA EXT	Gen.Purpose Logging	O	57h
WRITE LOG EXT	Gen.Purpose Logging	M	3Fh
WRITE LONG	Data Transfer		32h
WRITE LONG without Retry	Data Transfer		33h
WRITE MULTIPLE	Data Transfer	M	C5h
WRITE MULTIPLE EXT	48-bit Address	M	39h
WRITE MULTIPLE FUA EXT	48-bit Address	M	CEh
WRITE SECTOR(S)	Data Transfer	M	30h
WRITE SECTOR(S) (w/o retry)	Data Transfer	Obs	31h
WRITE SECTOR(S) EXT	48-bit Address	M	34h
WRITE UNCORRECTABLE EXT	General	O	45h

9.1 Identify Device

The processor within SSD responds to the ATA IDENTIFY DEVICE command with a pre-defined string of information on features, hardware and firmware revision information, and functionality support indicators.

Many portions of the IDENTIFY DEVICE response string are configurable at manufacturing time via the ConfigDriveUnique SCT diagnostic command.

IDENTIFY DEVICE Response Modification

Default IDENTIFY DEVICE information exists in advance of issuing a ConfigDriveUnique command. The processor implements a read-only mask (—FW Identify Maskǁ) which prevents changing of some elements of this default information. Details on modifying configurable IDENTIFY DEVICE information via the ConfigDriveUnique diagnostics command are found in the Diag/Mfg Firmware Specification.

9.2 Identify Device

The SSD drive supports ATA and SATA power management modes as listed below.

9.3 ATA Power Modes

The ATA power modes supported by the processor within the STM Plus series drive are:

- ACTIVE
- STANDBY
- IDLE
- SLEEP

9.4 SATA Link Power States

The SATA power states are as follows:

ACTIVE – PHY Ready, full power, Tx & Rx operational

PARTIAL – Reduced power, resumes in under 10 usec

SLUMBER – Reduced power, resumes in under 10 msec

The processor supports the following:

HIPM – Host-Initiated Power Management

DIPM – Device-Initiated Power Management

9.5 Power Mode Mapping

Table 13 Power Mode Mapping

Host Command Activity	ATA Power State	SATA Link Power Mode	
If DIPM Enabled		If DIPM Disabled	
No Activity	ACTIVE	Partial	Active
No Activity	IDLE (no auto-entry into IDLE)	Partial	Active
No Activity	STANDBY	Slumber	Active
No Activity	SLEEP	Slumber	Active

9.6 ATA Sleep Mode Behavior

For the processor, ATA SLEEP mode behavior is configurable via the ConfigDriveUnique diagnostics command (details are found in the Diag/Mfg Firmware Specification).
Default behavior is appropriate for drives that do not implement PAC signal power control:
Core power on; and
PHY “Slumber” setting; and
PLL bypass

Alternate behavior (configurable via ConfigDriveUnique diagnostics command) is optimized for maximum power saved in SLEEP state. This alternate behavior requires PAC signal power control to be implemented in external circuitry:
Core power off; and
PHY “Slumber” setting; and
PLL bypass

9.7 ATA IDLE Mode Behavior

For the SSD drive, ATA IDLE mode behavior is configurable via the ConfigDriveUnique diagnostics command (details are found in the Diag/Mfg Firmware Specification).
Default behavior is as follows:
PHY “Partial” setting
Alternate behaviors (configurable via ConfigDriveUnique diagnostics command) are as follows:
PHY “Slumber” setting
or
PHY “Slumber” setting; and
PLL bypass

10. S.M.A.R.T Support

10.1 Overview of S.M.A.R.T Support

Data storage drives capture a variety of information during operation that may be used to analyze drive “health.” Drive manufacturers have adopted S.M.A.R.T. (Self-Monitoring, Analysis, and Reporting Technology) to help warn system software, a system administrator, or a user of impending drive failure, while time remains to take preventive action. The technical documentation for S.M.A.R.T. is captured in the AT Attachment (ATA) standard. The standard defines the protocols for reporting errors and for invoking self-tests to collect and analyze data on demand. The ATA specification is flexible and provides for individual manufacturers to define their own unique vendor specific information. This section describes the baseline S.M.A.R.T. Commands and Attributes supported by the STM PLUS series processor. The information herein should be used in conjunction with the ATA standard and related documents, which may serve as references for topics and details not addressed here. Further, it is recommended to consult the list of public S.M.A.R.T. attributes.

10.2 S.M.A.R.T Command Set

Table 14 S.M.A.R.T command Set

Value (hex)	Command
00-CF	Reserved
D0	S.M.A.R.T. read attributes
D1*	S.M.A.R.T. read threshold
D2	S.M.A.R.T. enable/disable attribute autosave
D3*	S.M.A.R.T. save attribute values
D4	S.M.A.R.T. execute off-line immediate
D5	S.M.A.R.T. read log sector
D6	S.M.A.R.T. write log sector
D7*	S.M.A.R.T. write attribute threshold
D8	S.M.A.R.T. enable operations
D9	S.M.A.R.T. disable operations
DA	S.M.A.R.T. return status
DC-FF	Reserved (Vendor Specific)

* Note that D1, D3, and D7 have been obsolete in the ATA-8 specification.

10.3 Off-line Mode

The STM Plus series processor supports the optional 28-bit S.M.A.R.T. EXECUTION OFF-LINE IMMEDIATE (B0h/D4h) command per the ATA-8 specification. This command causes the processor to initiate the collection of S.M.A.R.T. data in an off-line mode and then preserve this data across power and reset events. Supported subcommands include those shown in the table below. Reference the ATA-8 specification for subcommand detail.

Table 15 S.M.A.R.T Execute Off-line Immediate Subcommands

Value	Description
00h	Execute S.M.A.R.T. off-line routine immediately in off-line mode
01h	Execute S.M.A.R.T. Short self-test routine immediately in off-line mode
02h	Execute S.M.A.R.T. Extended self-test routine immediately in off-line mode
04h	Execute S.M.A.R.T. Selective self-test routine immediately in off-line mode
7Fh	Abort off-line mode self-test routine
81h	Execute S.M.A.R.T. Short self-test routine immediately in captive mode
82h	Execute S.M.A.R.T. Extended self-test routine immediately in captive mode
84h	Execute S.M.A.R.T. Selective self-test routine immediately in

10.4 S.M.A.R.T Command Transport (SCT)

The STM PLUS series processor supports the S.M.A.R.T. Command Transport (SCT). SCT allows the host to send commands, send and receive data, and receive status to and from the processor using log page 0xE0 and log page 0xE1. SCT uses S.M.A.R.T. READ/WRITE LOG commands, READ/WRITE LOG EXT commands, or READ/WRITE LOG DMA EXT commands to access the log pages. For additional SCT information please reference ATA8-ACS.

10.5 S.M.A.R.T Command Transport (SCT)

The STM Plus series Processor provides diagnostic support via the SCT interface. The specific diagnostic support provided by processor firmware depends on the SSD requirements. Diagnostic and Manufacturing functions include:

- Low-level Format
- Configuring Drive-Unique options
- Configuring IDENTIFY DEVICE data
- Characterization and/or test of Flash memory array
- Physical Flash block accesses
- Error injection
- Error and S.M.A.R.T. log initialization, generation or extraction

- Retrieve internal Flash voltage levels, wear distributions, and identifiers
- Create and retrieve manufacturing record information
- Access external ISTWI (I2C-compatible) devices
- Other functions as necessary

11. Host Interface Configuration

11.1 Port Features and Capabilities

The STM Plus Series SATA Interface provides the following features

- Seamless SATA interoperability
- Plug-and-play field-proven SATA-v2.6-compliant interface
- 3 Gbps / 1.5 Gbps signaling (auto-negotiated)
- Native Command Queuing (NCQ) support
- S.M.A.R.T. command transport (SCT) technology
- SATA Signaling parameter configurability
- Spread-spectrum signaling support (5 KHz down spread)
- Tx/Rx pin swap capability (for PCB routing flexibility; see HRM for details)
- Host BIST FIS support

11.2 SATA PHY Configurations

The Snowbush Inc. 90nm-G SATA SAPIS PHY (SBSATA2000T90G) contains a number registers to customize various PHY attributes. Register addresses are two bytes (the upper byte identifies CMCU / channel and the lower byte the specific register). Register values are one byte.

11.3 Signaling Parameters

The STM Plus series processor includes flexible signal parameter control for both transmit and receive paths.

The transmit path provides the following control:

Output Amplitude: 375-1000mVpp differential (5-bit programmable steps)

Output Slew Rate: 85-110ps (8 steps programmable)

Output Pre-emphasis (4-bit programmable steps)

Spread Spectrum Generation

The receive path provides the following control:

Signal Detect Threshold: 50-225 mVpp (8 steps programmable)

Supports spread spectrum signaling

11.4 PHY Register Addresses and Definitions

The PHY register addresses and definitions are described in the following tables.

Table 16 PHY TX Register Definition

Signal Name	Lower Byte ADDR	Default Value	Description	
TX_AMPL	0x05	5'b00000	Channel TX amplitude 5'b00000 – 97mV 5'b00001 – 144mV 5'b00010 – 191mV 5'b00011 – 237mV 5'b00100 – 282mV 5'b00101 – 327mV 5'b00110 – 371mV 5'b00111 – 415mV 5'b01000 – 459mV 5'b01001 – 502mV 5'b01010 – 544mV 5'b01011 – 586mV 5'b01100 – 627mV 5'b01101 – 666mV 5'b01110 – 705mV 5'b01111 – 742mV	5'b10000 – 779mV 5'b10001 – 814mV 5'b10010 – Reserved 5'b10011 – Reserved 5'b10100 – Reserved 5'b10101 – Reserved 5'b10110 – Reserved 5'b10111 – Reserved 5'b11000 – Reserved 5'b11001 – Reserved 5'b11010 – Reserved 5'b11011 – Reserved 5'b11100 – Reserved 5'b11101 – Reserved 5'b11110 – Reserved 5'b11111 – Reserved
TX_SLEW	0x00	3'b000	TX_SLEW_C= 1'b0 3'b000 – 58ps 3'b001 – 66ps 3'b010 – 75ps 3'b011 – 85ps TX_SLEW_C= 1'b1 3'b000 – 101ps 3'b001 – 112ps 3'b010 – 127ps 3'b011 – 140ps	3'b100 – 94ps 3'b101 – 104ps 3'b110 – 112ps 3'b111 – 119ps 3'b100 – 151ps 3'b101 – 162ps 3'b110 – 170ps 3'b111 – 179ps
TX_SLEW_C	0x1A	1'b0	TX driver coarse slew rate select. See TX_SLEW above for functionality.	
TX_EMPH	0x2B	3'b000	TX driver emphasis select 3'b000 – 0dB	3'b100 – Reserved 3'b101 – Reserved

			3'b001 – -1.0dB (11%) 3'b010 – -2.2dB (22%) 3'b011 – -3.5dB (33%)	3'b110 – Reserved 3'b111 – Reserved

Table 17 PHY RX Register Definition

Signal Name	Lower Byte ADDR	Default Value	Description	
Sd_thset	0x03	3'b101	Channel signal detect threshold setting. 3'b000 – 225mV 3'b001 – 200mV 3'b010 – 175mV 3'b011 – 150mV	 3'b100 – 125mV 3'b101 – 100mV 3'b110 – 75mV 3"b111 – 50mv

11.5 PHY Configuration Workflow

In order to alter the PHY settings, the host shall be capable of:

1. Read all of the PHY registers
2. Write all or some of the PHY registers temporarily (until power cycle / chassis reset)
3. Write all or some of the PHY registers immediately and save them for subsequent use

The format of the data will be a series of 16-bit words following the convention described in [ATA- 8] (section 3.2.8). The contents of the data will be a header {NumRecords, Reserved} followed by NumRecords sets of {Offset, RegValue} (Figure 3).

Table 18 SCT Read/Write PHY data format

Word	Description
0	Number of records
1	Reserved
2	Register offset
3	15:8 00h = Reserved 7:0 Register value
4	Register offset
5	15:8 00h = Reserved 7:0 Register value
…	…

The workflow that will be used to read and write the PHY registers is given below.

Host Actions for Read PHY:

1. Send Command:
   a. Issue a S.M.A.R.T. WRITE LOG command with LBA = E0h (SCT Command/Status Log Address).
   b. Write one sector of data (key data block) specifying a “Read PHY” command {action code = C004h (vendor specific) and function code = 0}.

2. Read Status:

a. Issue a S.M.A.R.T. READ LOG command with LBA = E0h (SCT Command/Status Log Address). Verify that device is ready to transfer data – this may have to be done multiple times.

3. Read Data:

a. Issue a S.M.A.R.T. READ LOG command with LBA = E1h (SCT Data Transfer Log Address), Count = 2. This shall return all the current PHY register settings. Two sectors of data shall be returned. The data after the end of the register settings shall contain zeros.

4. Read Status:
   a. Issue a S.M.A.R.T. READ LOG command with LBA = E0h (SCT Command/Status Log Address). Verify that data was transferred successfully.

Host Actions for Write PHY (Temp / Save):

1. Send Command:

   a. Issue a S.M.A.R.T. WRITE LOG command with LBA = E0h (SCT Command/Status Log Address).

   b. Write one sector of data (key data block) specifying a “Write PHY Temp / Save” command {action code = C004h (vendor specific) and function code = 1 (for Temp) or 2 (for Save)}.

2. Read Status:

   a. Issue a S.M.A.R.T. READ LOG command with LBA = E0h (SCT Command/Status Log Address). Verify that device is ready to accept data.

3. Write Data:

   a. Issue a S.M.A.R.T. WRITE LOG command with LBA = E1h (SCT Data Transfer Log

Address), Count = 1 or 2 (depending upon how many registers are to be set). Write the desired PHY register settings. The number of sectors transferred depends upon whether the host would like to specify all or only some register values. The data after the end of the register settings shall contain zeros.

4. Read Status:

a. Issue a S.M.A.R.T. READ LOG command with LBA = E0h (SCT Command/Status Log Address). This may have to be done repeatedly to:

1) Verify that the data was transferred successfully.

2) Verify that the settings were saved successfully (if command is “Write PHY Save”).

3) Verify whether all / some / none of the settings were applied successfully.

4) Verify whether the command is complete or pending - the command will not indicate 'done' until the data is transferred, saved and applied.

11.6 SATA BIST Support

SATA BIST is supported per the Serial ATA standard, v2.6. Support includes BIST FIS for Host initiated BIST modes.

Entry into a desired test mode requires delivery of a BIST Activate FIS from the Application layer. Since BIST Activate FIS is bidirectional, either the Host or the Drive may initiate entry into a specific BIST operating mode. STM PLUS series SSD supports the following BIST modes (the BIST Activate FIS pattern definition bit(s) are shown in parenthesis):

1. Far End Retimed Loopback (L)
2. Far End Transmit Only (T)

a) With ALIGN primitives and scrambled data (T)
b) With ALIGN primitives and without scrambled date (T + S)
c) Without ALIGN primitives and scrambled date (T + A)
d) Without ALIGN primitives and without scrambled date (T + A + S)

When the Far End Transmit Only BIST mode is selected (modes 2a – 2d above), the STM PLUS processor will continually transmit the contents of the BIST Activate FIS DATA1 (Dword One) and DATA2 (Dword Two). See section 14.2 for some commonly used DATA1 and DATA2 patterns.

Non-Compliant Patterns

Non-compliant patterns are continuously repeated encoded values that are not presented in a standard data FIS format. Non-compliant test patterns are intended to satisfy a number of testing needs including jitter measurement, electrical parameter tests, and signal quality assessment. Some commonly used non-compliant patterns include:

High-frequency test pattern (HFTP)
Medium-frequency test pattern (MFTP)
Low-frequency test pattern (LFTP)
“Lone-Bit” pattern with negative disparity (LBP-)
“Lone-Bit” pattern with positive disparity (LBP+)
SATA Transmitter Jitter (SXJT)

These patterns may be coded using two DWORDs in the BIST Activate FIS as illustrated in the table below:

Table 19 Typical non-compliant BIST Patterns

Abbr	Description	Pattern
LFTP	Std. non-compliant Low Frequency Test Pattern	0x7E7E7E7E_7E7E7E7E
MFTP	Std. non-compliant Mid Frequency Test Pattern	0x78787878_78787878
HFTP	Std. non-compliant High Frequency Test Pattern	0x4A4A4A4A_4A4A4A4A
LBP-	Std. non-compliant Lone-Bit (–disparity) Test Pattern	0x0C8B0C8B_0C8B0C8B
LBP+	Std. non-compliant Lone-Bit (+disparity) Test Pattern	0x8B0C8B0C_8B0C8B0C
SXJT	SATA Transmitter Jitter	0xF4EBF4EB_78064AF5

Compliant Patterns

The STM Plus processor supports a host-transmitted compliant BIST pattern when it is placed into the Far End Retimed Loopback BIST mode.

Far End Setup

When the STM Plus processor receives a far-end BIST FIS, they return the R_OK primitive to notify the Host that the FIS has been successfully received. The processor then evaluates the Pattern Definition and places the transport, link, and physical layers into the mode required to transmit the requested data stream.

12. Contact Information

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